A. CHEHAB DEPARTMENT OF ELECTRICAL AND COMPUTER EGINEERING
M. MANSOUR AMERICAN UNIVERSITY OF BEIRUT

FALL TERM 2005-2006

MIDTERM I

EECE320 - DIGITAL SYTEMS DESIGN

NOVEMBER 24, 2005

NAME: _____ ID: _____

COURSE SECTION: SECTION 1 (PROF. CHEHAB)

SECTIONS 2 & 3 (PROF. MANSOUR)

INSTRUCTIONS:

- **THE EXAM IS CLOSED BOOK/CLOSED NOTES. THE DURATION IS 1.5 HOURS.**
- **CALCULATORS ARE NOT ALLOWED.**
- **WRITE YOUR NAME AND ID NUMBER IN THE SPACE PROVIDED ABOVE.**
- **INDICATE THE SECTION YOU ARE REGISTERED IN.**
- **PROVIDE YOUR ANSWERS IN THE SPACE PROVIDED ON THE QUESTION SHEET.**
- **THE SCRATCH BOOKLET WILL NOT BE CONSIDERED IN GRADING.**
- **BE AS NEAT AND CLEAR AS POSSIBLE.**

Problem	Total Points	Earned Points
1	6	
2	6	
3	6	
4	6	
5	8	
6	8	
7	12	
8	16	
9	12	
10	10	
11	10	
Total	100	

Problem 1: [6 points]

Find the base b in the case where: $(859)_{10} = (5B7)_b$

B = _____

Problem 2: [6 points]

Perform the operation $87 - 99$ in two's complement representation using 8 bits.

Problem 3: [6 points]

Find the radix complement and the diminished radix complement for the number $(4723)_8$.

Radix complement = _____ Diminished radix complement = _____

Problem 4: [6 points]

How many minterms are included in the following 4-variable function and what are they?

$$\mathbf{F(A,B,C,D) = ((A+B)' + (C+D)')'}$$

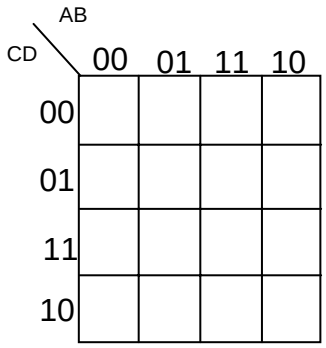
The minterms are: _____

_____

Problem 5: [8 points]

Consider the function: F = A'B'C'D' + A'B'C'D + A'B'CD + A'B'CD' + A'BCD'+
ABC'D + ABCD' + AB'C'D' +AB'CD'

a) Mark the distinguished-1 cells on the map.



b) What is a minimum SOP expression for F?

_____

Problem 6: [8 points]

Draw the gate implementation of the expression F = $(X_1+X_2')(X_2+X_3)$

a) What type of hazard is possible with this implementation?

_____

b) Indicate which transition causes such hazard

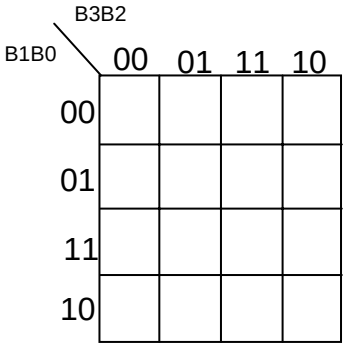
_____

c) How do you modify the implementation to obtain a hazard-free circuit?

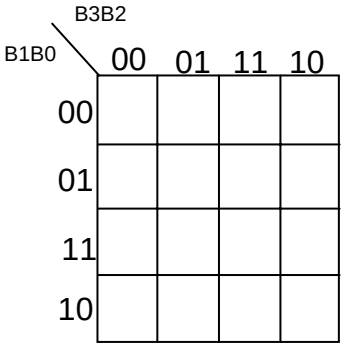
Problem 7: [12 points]

Design a circuit to convert from BCD to EXCESS-3 representation. Start by filling out the truth table, then fill the K-maps, then minimize the expressions for E3, E2, E1, and E0.

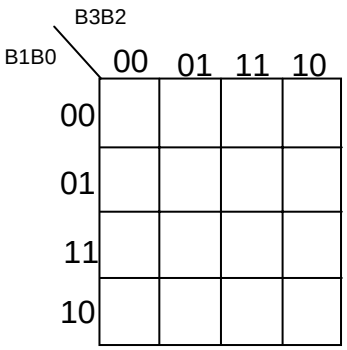
B3	B2	B1	B0	E3	E2	E1	E0
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				



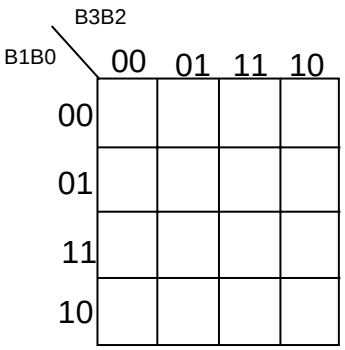
E3 = _____



E2 = _____



E1 = _____



E0 = _____

Problem 8: [**16 points**]

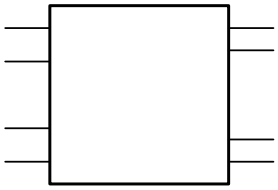
Write a VHDL entity and **behavioral** architecture for a circuit that perform the conversion indicated in the previous problem. The circuit has inputs (B3, B2, B1, B0) and outputs (E3, E2, E1, E0). In addition, it has an active-low enable signal (EN_L). Then, write a testbench to the test your circuit with the following combinations:

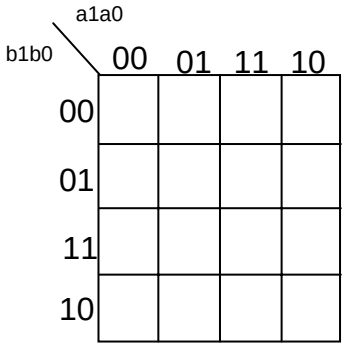
EN_L = 1, B3B2B1B0 = 0110
EN_L = 0, B3B2B1B0 = 0111
EN_L = 0, B3B2B1B0 = 1000
EN_L = 0, B3B2B1B0 = 1001

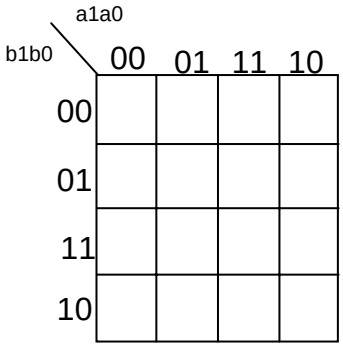
Problem 9: Binary Sorting [**12 points**]

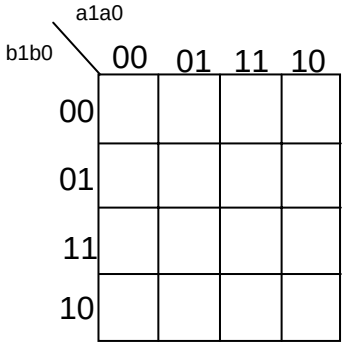
Let **A**=$\mathbf{a_1a_0}$ and **B**=$\mathbf{b_1b_0}$ be two unsigned 2-bit binary numbers.

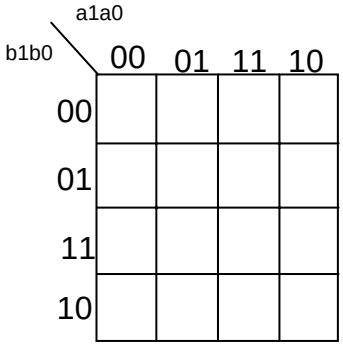
a) Design a logic circuit that sorts the two inputs, putting the maximum at the top output and the minimum at the bottom output, i.e., **MX**=$\mathbf{mx_1mx_0}$=max(**A**,**B**), and **MN**= $\mathbf{mn_1mn_0}$=min(**A**,**B**). Write down Boolean equations and draw the logic diagram.





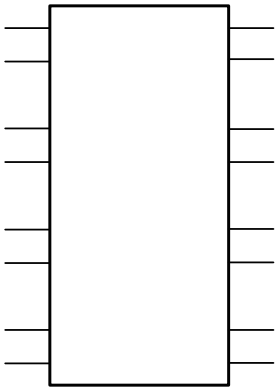






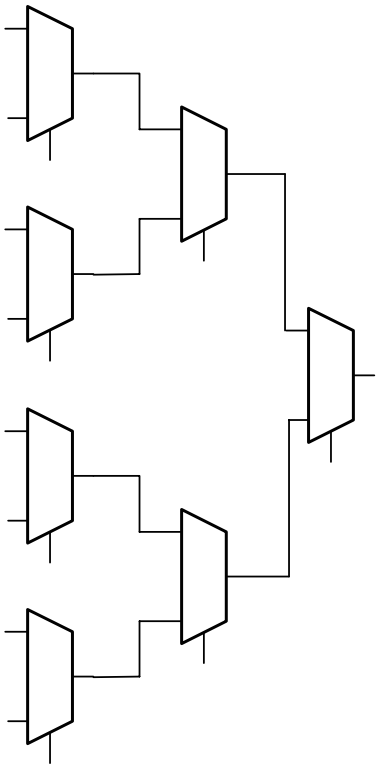
(**Problem 9(a) cont'd**)

b) Using the block that you designed in part a), design a logic circuit that sorts four unsigned 2-bit binary numbers **A**=$\mathbf{a_1a_0}$, **B**=$\mathbf{b_1b_0}$, **C**=$\mathbf{c_1c_0}$, **D**=$\mathbf{d_1d_0}$ in descending order, putting the maximum at the top and the minimum at the bottom, i.e., **MAX** ≥ **M3** ≥ **M2** ≥ **MIN**. Label all connections clearly.



Problem 10: Multiplexer function [**10 points**]

What Boolean function *F*(*A*,*B*,*C*,*D*) does the following circuit implement? Write your answer as a canonical POS expression.



F = _____

Problem 11: 4-to-16 Decoder [**10 points**]

In this problem, you are asked to design a 4-to-16 decoder with enable as shown below. You have available **only two** 2-to-4 decoders with enable and **active-low** outputs, and a set of NOR gates. Show how to design the 4-to-16 decoder using two 2-to-4 decoders and NOR gates. Label all your connections clearly.